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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,083	TOPHAM, NIGEL PETER	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/16/08*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims, 1,2 and 4-15 (as dependent on claim 1),22,24-26, and 28 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-15, 22,24-26,28 of prior U.S. Patent No. 6,754,8706. This is a double patenting rejection. The corresponding claims are shown side by side below

Instant application	Patent No. 6,754,806
1. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising: a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; a second	1. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising: a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; a second

Instant application	Patent No. 6,754,806
(claim 1 continued) candidate output value producing unit connected for receiving said input value and operable, during operation of said first candidate output value producing unit to produce said first candidate output value, to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; an in-range value determining unit which determines which one of said first and second candidate output values is within said preselected output-value range; and an output value selection unit which selects as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.	(claim 1 continued) candidate output value producing unit connected for receiving said input value and operable, during operation of said first candidate output value producing unit to produce said first candidate output value, to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; an in-range value determining unit which determines which one of said first and second candidate output values is within said preselected output-value range; and an output value selection unit which selects as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.

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2. Mapping circuitry as claimed in claim 1, wherein said in-range value determining unit is operable to determine which one of said first and second candidate output values is within said preselected output-value range during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.	2. Mapping circuitry as claimed in claim 1, wherein said in-range value determining unit is operable to determine which one of said first and second candidate output values is within said preselected output-value range during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.
4. Mapping circuitry as claimed in claim 1 or 3, further comprising: an input range determining unit connected for receiving said input value and operable to determine whether said input value is within said preselected input-value range; and a third candidate output value producing unit which produces a third candidate output value; wherein said output value selection unit is operable, when said input range determining unit determines that said input value is outside said preselected input-value range, to select as said corresponding output value said third candidate output value.	4. Mapping circuitry as claimed in claim 1 or 3, further comprising: an input range determining unit connected for receiving said input value and operable to determine whether said input value is within said preselected input-value range; and a third candidate output value producing unit which produces a third candidate output value; wherein said output value selection unit is operable, when said input range determining unit determines that said input value is outside said preselected input-value range, to select as said corresponding output value said third candidate output value.

Instant application	Patent No. 6,754,806
5. Mapping circuitry as claimed in claim 4, wherein said third candidate output value producing unit is connected for receiving said input value and said third candidate output value is dependent upon said input value.	5. Mapping circuitry as claimed in claim 4, wherein said third candidate output value producing unit is connected for receiving said input value and said third candidate output value is dependent upon said input value.
6. Mapping circuitry as claimed in claim 5, wherein said third candidate output value is equal to said input value.	6. Mapping circuitry as claimed in claim 5, wherein said third candidate output value is equal to said input value.
7. Mapping circuitry as claimed in claim 4, wherein said input range determining unit is operable to determine whether said input value is outside said preselected input-value range during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.	7. Mapping circuitry as claimed in claim 4, wherein said input range determining unit is operable to determine whether said input value is outside said preselected input-value range during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.
8. Mapping circuitry as claimed in claim 4, wherein said third candidate output value producing unit is operable to produce said third	8. Mapping circuitry as claimed in claim 4, wherein said third candidate output value producing unit is operable to produce said third

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candidate output value during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.	candidate output value during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.
9. Mapping circuitry as claimed in claim 1 or 3, wherein at least one of said output-range limit values is variable during operation of the circuitry.	9. Mapping circuitry as claimed in claim 1 or 3, wherein at least one of said output-range limit values is variable during operation of the circuitry.
10. Mapping circuitry as claimed in claim 1 or 3, wherein the span of the preselected output-value range is greater than the span of the preselected input-value range.	10. Mapping circuitry as claimed in claim 1 or 3, wherein the span of the preselected output-value range is greater than the span of the preselected input-value range.
11. Mapping circuitry as claimed in claim 4, wherein said input range determining unit is operable to determine whether said input value is outside said preselected input-value range by producing a detection value that differs by a third offset value from the received input value, and detecting when a predetermined bit of the detection value has a predetermined logic value.	11. Mapping circuitry as claimed in claim 4, wherein said input range determining unit is operable to determine whether said input value is outside said preselected input-value range by producing a detection value that differs by a third offset value from the received input value, and detecting when a predetermined bit of the detection value has a predetermined logic value.

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12. Mapping circuitry as claimed in claim 11, wherein said third offset value is set in dependence upon an input-range limit value defining one of the limits of the predetermined input-value range.	12. Mapping circuitry as claimed in claim 11, wherein said third offset value is set in dependence upon an input-range limit value defining one of the limits of the predetermined input-value range.
13. Mapping circuitry as claimed in claim 12, wherein the detection value is produced by adding the third offset value to the received input value.	13. Mapping circuitry as claimed in claim 12, wherein the detection value is produced by adding the third offset value to the received input value.
14. Mapping circuitry as claimed in claim 11, wherein said predetermined bit is the most significant bit of the produced detection value.	14. Mapping circuitry as claimed in claim 11, wherein said predetermined bit is the most significant bit of the produced detection value.
15. Mapping circuitry as claimed in claim 1 or 3, further comprising an offset varying unit operable selectively to vary said first and second offset values during operation of the circuitry, whilst maintaining said difference between them.	15. Mapping circuitry as claimed in claim 1 or 3, further comprising an offset varying unit operable selectively to vary said first and second offset values during operation of the circuitry, whilst maintaining said difference between them.

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22. A processor comprising: an instruction issuing unit which issues instructions; at least one instruction executing unit which executes the issued instructions; a register file, having a plurality of physical registers; and mapping circuitry which maps an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said input value being a logical register identifier specified by one of said instructions, and said output value being a physical register identifier used for identifying one of the physical registers within said register file that corresponds to the specified logical register identifier; wherein said mapping circuitry comprises: a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; a	22. A processor comprising: an instruction issuing unit which issues instructions; at least one instruction executing unit which executes the issued instructions; a register file, having a plurality of physical registers; and mapping circuitry which maps an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said input value being a logical register identifier specified by one of said instructions, and said output value being a physical register identifier used for identifying one of the physical registers within said register file that corresponds to the specified logical register identifier; wherein said mapping circuitry comprises: a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; a second candidate output value

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(claim 22 continued) second candidate output value producing unit connected for receiving said input value and operable, during operation of said first candidate output value producing unit to produce said first candidate output value, to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; an in-range value determining unit which determines which one of said first and second candidate output values is within said preselected output-value range; and an output value selection unit	(Claim 22 continued) second candidate output value producing unit connected for receiving said input value and operable, during operation of said first candidate output value producing unit to produce said first candidate output value, to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; an in-range value determining unit which determines which one of said first and second candidate output values is within said preselected output-value range; and an output value selection unit

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(Claim 22 continued) which selects as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.	(claim 22 continued) which selects as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.
24. A processor as claimed in claim 22 or 23, wherein said register file comprises a dynamically-named region and mapping-circuitry output values within the predetermined output-value range provide said physical register identifiers of those physical registers within said dynamically-named region.	24. A processor as claimed in claim 22 or 23, wherein said register file comprises a dynamically-named region and mapping-circuitry output values within the predetermined output-value range provide said physical register identifiers of those physical registers within said dynamically-named region.
25. A processor as claimed in claim 22 or 23, wherein said register file comprises a statically-named region and mapping-circuitry output values outside the predetermined output-value range provide said physical register identifiers of those physical registers within said statically-named region.	25. A processor as claimed in claim 22 or 23, wherein said register file comprises a statically-named region and mapping-circuitry output values outside the predetermined output-value range provide said physical register identifiers of those physical registers within said statically-named region.
26. A mapping method for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected	26. A mapping method for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected

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(claim 26 continued) range of allowable output values, said method comprising: producing a first candidate output value that differs by a first offset value from the received input value; producing, during production of said first candidate output value, a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; determining which one of said first and second candidate output values is within said preselected output-value range; and selecting as said corresponding output value	(claim 26 continued) range of allowable output values, said method comprising: producing a first candidate output value that differs by a first offset value from the received input value; producing, during production of said first candidate output value, a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; determining which one of said first and second candidate output values is within said preselected output-value range; and selecting as said corresponding output value

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(claim 26 continued) that one of said first and second candidate output values which is determined to be within said output-value range.	(claim 26 continued) that one of said first and second candidate output values which is determined to be within said output-value range.
28. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising: first candidate output value producing means connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; second candidate output value producing means connected for receiving said input value and operable, during operation of said first candidate output value producing means to produce said first candidate output value, to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value	28. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising: first candidate output value producing means connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; second candidate output value producing means connected for receiving said input value and operable, during operation of said first candidate output value producing means to produce said first candidate output value, to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value

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(Claim 28 continued) range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; in-range value determining means for determining which one of said first and second candidate output values is within said preselected output-value range; and output value selection means for selecting as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.	(claim 28 continued) range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; in-range value determining means for determining which one of said first and second candidate output values is within said preselected output-value range; and output value selection means for selecting as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 3,4-15(as dependent on claim 3)16-21, 23 and 24-25 (as dependent of claim 23),27, and 29 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 3-21,23-26,27,29 of U.S. Patent No. 6,754,806. Although the conflicting claims are not identical, they are not patentably distinct from each other because first of all the similarities and differences are shown in the side by side showing of the claims below.

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3. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising: a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; a second candidate output value producing unit connected for receiving said input value and operable	3. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising: a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; a second candidate output value producing unit connected for receiving said input value and operable

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,during operation of said first candidate output value producing unit to produce said first candidate output value, to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; an in-range value determining unit operable to determine, during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values, which one of said first and second	to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; an in-range value determining unit operable to determine, during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values, which one of said first and second

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candidate output values is within said preselected output-value range; and an output value selection unit which selects as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.	candidate output values is within said preselected output-value range; and an output value selection unit which selects as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.
4. Mapping circuitry as claimed in claim 1 or 3, further comprising: an input range determining unit connected for receiving said input value and operable to determine whether said input value is within said preselected input-value range; and a third candidate output value producing unit which produces a third candidate output value; wherein said output value selection unit is operable, when said input range determining unit determines that said input value is outside said preselected input-value range, to select as said corresponding output value said third candidate output value.	4. Mapping circuitry as claimed in claim 1 or 3, further comprising: an input range determining unit connected for receiving said input value and operable to determine whether said input value is within said preselected input-value range; and a third candidate output value producing unit which produces a third candidate output value; wherein said output value selection unit is operable, when said input range determining unit determines that said input value is outside said preselected input-value range, to select as said corresponding output value said third candidate output value.

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5. Mapping circuitry as claimed in claim 4, wherein said third candidate output value producing unit is connected for receiving said input value and said third candidate output value is dependent upon said input value.	5. Mapping circuitry as claimed in claim 4, wherein said third candidate output value producing unit is connected for receiving said input value and said third candidate output value is dependent upon said input value.
6. Mapping circuitry as claimed in claim 5, wherein said third candidate output value is equal to said input value.	6. Mapping circuitry as claimed in claim 5, wherein said third candidate output value is equal to said input value.
7. Mapping circuitry as claimed in claim 4, wherein said input range determining unit is operable to determine whether said input value is outside said preselected input-value range during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.	7. Mapping circuitry as claimed in claim 4, wherein said input range determining unit is operable to determine whether said input value is outside said preselected input-value range during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.
8. Mapping circuitry as claimed in claim 4, wherein said third candidate output value producing unit is	8. Mapping circuitry as claimed in claim 4, wherein said third candidate output value producing unit is

Instant application	Patent No. 6,754,806
operable to produce said third candidate output value during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.	operable to produce said third candidate output value during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values.
9. Mapping circuitry as claimed in claim 1 or 3, wherein at least one of said output-range limit values is variable during operation of the circuitry.	9. Mapping circuitry as claimed in claim 1 or 3, wherein at least one of said output-range limit values is variable during operation of the circuitry.
10. Mapping circuitry as claimed in claim 1 or 3, wherein the span of the preselected output-value range is greater than the span of the preselected input-value range.	10. Mapping circuitry as claimed in claim 1 or 3, wherein the span of the preselected output-value range is greater than the span of the preselected input-value range.
11. Mapping circuitry as claimed in claim 4, wherein said input range determining unit is operable to determine whether said input value is outside said preselected input-value range by producing a detection value that differs by a third offset value from the received input value, and detecting when a	11. Mapping circuitry as claimed in claim 4, wherein said input range determining unit is operable to determine whether said input value is outside said preselected input-value range by producing a detection value that differs by a third offset value from the received input value, and detecting when a

Instant application	Patent No. 6,754,806
predetermined bit of the detection value has a predetermined logic value.	predetermined bit of the detection value has a predetermined logic value.
12. Mapping circuitry as claimed in claim 11, wherein said third offset value is set in dependence upon an input-range limit value defining one of the limits of the predetermined input-value range.	12. Mapping circuitry as claimed in claim 11, wherein said third offset value is set in dependence upon an input-range limit value defining one of the limits of the predetermined input-value range.
13. Mapping circuitry as claimed in claim 12, wherein the detection value is produced by adding the third offset value to the received input value.	13. Mapping circuitry as claimed in claim 12, wherein the detection value is produced by adding the third offset value to the received input value.
14. Mapping circuitry as claimed in claim 11, wherein said predetermined bit is the most significant bit of the produced detection value.	14. Mapping circuitry as claimed in claim 11, wherein said predetermined bit is the most significant bit of the produced detection value.
15. Mapping circuitry as claimed in claim 1 or 3, further comprising an offset varying unit operable selectively to vary said first and second offset values during operation of the circuitry, whilst maintaining said difference between them.	15. Mapping circuitry as claimed in claim 1 or 3, further comprising an offset varying unit operable selectively to vary said first and second offset values during operation of the circuitry, whilst maintaining said difference between them.

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16. Mapping circuitry as claimed in claim 1 or 3, wherein said in-range value determining unit is operable to produce a detection value that differs by an in-range offset value from the received input value, and to determine that the in-range output value is the first candidate output value when a preselected bit of the produced detection value has a first logic value and that the in-range output value **is** the second candidate output value when that bit has a second logic value.	16. Mapping circuitry as claimed in claim 1 or 3, wherein said in-range value determining unit is operable to produce a detection value that differs by an in-range offset value from the received input value, and to determine that the in-range output value is the first candidate output value when a preselected bit of the produced detection value has a first logic value and that the in-range **candidate** output value as the second candidate output value when that bit has a second logic value.
17. Mapping circuitry as claimed in claim 16, wherein said in-range offset value differs from the first offset value by one of said output-range limit values and differs from the second offset value by the other of said output-range limit values.	17. Mapping circuitry as claimed in claim 16, wherein said in-range offset value differs from the first offset value by one of said output-range limit values and differs from the second offset value by the other of said output-range limit values.
18. Mapping circuitry as claimed in claim 16, further comprising an offset varying unit operable selectively to vary said first and second offset values during operation of the circuitry, whilst maintaining	18. Mapping circuitry as claimed in claim 16, further comprising an offset varying unit operable selectively to vary said first and second offset values during operation of the circuitry, whilst maintaining

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said difference between them, and wherein said offset varying unit also varies said in-range offset value when said first and second offset values are varied so as to leave unchanged the respective differences between the first and in-range offset values and between the second and in-range offset values.	said difference between them, and wherein said offset varying unit also varies said in-range offset value when said first and second offset values are varied so as to leave unchanged the respective differences between the first and in-range offset values and between the second and in-range offset values.
19. Mapping circuitry as claimed in claim 16, wherein the in-range offset value is dependent upon an input-range limit value defining one of the limits of the preselected input-value range.	19. Mapping circuitry as claimed in claim 16, wherein the in-range offset value is dependent upon an input-range limit value defining one of the limits of the preselected input-value range.
20. Mapping circuitry as claimed in claim 18, wherein the detection value is produced by adding the in-range offset value to the received input value.	20. Mapping circuitry as claimed in claim 18, wherein the detection value is produced by adding the in-range offset value to the received input value.
21. Mapping circuitry as claimed in claim 16, wherein said preselected bit is the most significant bit of the produced detection value.	21. Mapping circuitry as claimed in claim 16, wherein said preselected bit is the most significant bit of the produced detection value.

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23. A processor comprising: an instruction issuing unit which issues instructions; at least one instruction executing unit which executes the issued instructions; a register file, having a plurality of physical registers; and mapping circuitry which maps an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said input value being a logical register identifier specified by one of said instructions, and said output value being a physical register identifier used for identifying one of the physical registers within said register file that corresponds to the specified logical register identifier; wherein said mapping circuitry comprises: a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; a second candidate output value producing unit connected for receiving said input value and operable	23. A processor comprising: an instruction issuing unit which issues instructions; at least one instruction executing unit which executes the issued instructions; a register file, having a plurality of physical registers; and mapping circuitry which maps an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said input value being a logical register identifier specified by one of said instructions, and said output value being a physical register identifier used for identifying one of the physical registers within said register file that corresponds to the specified logical register identifier; wherein said mapping circuitry comprises: a first candidate output value producing unit connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; a second candidate output value producing unit connected for receiving said input value and operable

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(claim 23 continued) **, during operation of said first candidate output value producing unit to produce said first candidate output value** to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; an in-range value determining unit operable to determine, during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values, which one of said first and second candidate output values is within said preselected output-	(claim 23 continued) to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; an in-range value determining unit operable to determine, during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values, which one of said first and second candidate output values is within said preselected output-

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(claim 23 continued) value range; and an output value selection unit which selects as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.	(claim 23 continued) value range; and an output value selection unit which selects as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.
24. A processor as claimed in claim 22 or 23, wherein said register file comprises a dynamically-named region and mapping-circuitry output values within the predetermined output-value range provide said physical register identifiers of those physical registers within said dynamically-named region.	24. A processor as claimed in claim 22 or 23, wherein said register file comprises a dynamically-named region and mapping-circuitry output values within the predetermined output-value range provide said physical register identifiers of those physical registers within said dynamically-named region.
25. A processor as claimed in claim 22 or 23, wherein said register file comprises a statically-named region and mapping-circuitry output values outside the predetermined output-value range provide said physical register identifiers of those physical registers within said statically-named region.	25. A processor as claimed in claim 22 or 23, wherein said register file comprises a statically-named region and mapping-circuitry output values outside the predetermined output-value range provide said physical register identifiers of those physical registers within said statically-named region.
27. A mapping method for mapping an input value, within a preselected range of allowable input values, to a	27. A mapping method for mapping an input value, within a preselected range of allowable input values, to a

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(claim 27 continued) corresponding output value within a preselected range of allowable output values, said method comprising: producing a first candidate output value that differs by a first offset value from the received input value; producing,**during production of said first candidate output value,** a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; determining, during production of one or both of said first and second candidate output values, which one of said first and second candidate output values is within said preselected output-value range; and	(claim 27 continued) corresponding output value within a preselected range of allowable output values, said method comprising: producing a first candidate output value that differs by a first offset value from the received input value; producing a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; determining, during production of one or both of said first and second candidate output values, which one of said first and second candidate output values is within said preselected output-value range; and

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(claim 27 continued) selecting as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.	(claim 27 continued) selecting as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.
29. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising: first candidate output value producing means connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; second candidate output value producing means connected for receiving said input value and **, during operation of said first candidate output value producing means to produce said first candidate output value** operable to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective	29. Mapping circuitry for mapping an input value, within a preselected range of allowable input values, to a corresponding output value within a preselected range of allowable output values, said circuitry comprising: first candidate output value producing means connected for receiving said input value and operable to produce a first candidate output value that differs by a first offset value from the received input value; second candidate output value producing means connected for receiving said input value and operable to produce a second candidate output value that differs by a second offset value from the received input value, the first and second offset values being such that a difference between them is equal to a difference between respective

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(claim 29 continued) output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; in-range value determining means operable to determine, during operation of one or both of said first and second candidate value producing means to produce said first and second candidate output values, which one of said first and second candidate output values is within said preselected output-value range; and output value selection means for selecting as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.	(claim 29 continued) output-range limit values defining the limits of the preselected output-value range and such that, for any said input value within said preselected input-value range, one of the first and second candidate output values is within the preselected output-value range and the other of those two values is outside that range; in-range value determining means operable to determine, during operation of one or both of said first and second candidate value producing means to produce said first and second candidate output values, which one of said first and second candidate output values is within said preselected output-value range; and output value selection means for selecting as said corresponding output value that one of said first and second candidate output values which is determined to be within said output-value range.

As to the addition of the claim language (second candidate output value producing unit…during operation of said first candidate output value producing unit to produce said first candidate output) in independent claim 3 and independent claim 23 and independent claim 29 as well as the claim language (producing during production of the first candidate value, a second candidate output value in claim 27) these claimed versions of the this feature in the instant application is obvious in view of the claim language of claim 7 of the patent including "during operation of one or both of said first and second candidate value producing units to produce said first and second candidate output values". Consequently the first and second candidate units in at least one claimed embodiment concurrently operated to produce the respective first and second candidate outputs. Also as to claim 16, the changing the name of the output value by deleting an adjective (or changing "as" to "is") does not change the structure or operation and therefore this feature would have been obvious in view of the patent.

Response to Arguments

Applicant's arguments, see amendment , filed 1/16/08, with respect to the rejection(s) of claim(s) 1-29 under 35 U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of patent No. 6,754,806.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC
/Eric Coleman/
Primary Examiner, Art Unit 2183